AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application. Applicants respectfully submit that no new matter has been added by the instant amendment to the claims.

Listing of Claims:

1. (Currently Amended) An [[A]]adjustment device [[(1)]] for adjusting at least one control device [[(2)]] with at least one control device microcontroller [[(3)]] and with at least one control device debug interface [[(4)]], ~~where the adjustment device (1) comprises~~ comprising:

at least one programmable unit [[(5)]];

at least one data transmission interface [[(6)]] for connecting the adjustment device [[(1)]] to an operating unit [[(7),]]; ~~and~~

at least one adjustment device debug interface [[(8)]] for connecting the adjustment device [[(1)]] to the control device debug interface [[(4)]] of the control device [[(2),]]; and

~~characterized by the fact that~~

~~the adjustment device [[(1)]] comprises in addition~~ at least one memory [[(9)]] for at least one address list [[(11)]] and at least one data list [[(12)]], where the addresses stored in the address list [[(11)]] denote memory locations in the address space [[(10)]] of the control device microcontroller [[(3)]] and where with the use of the adjustment device debug interface [[(8)]] data from the memory locations which are in the address space [[(10)]] of the control device microcontroller [[(3)]] and which are determined by the contents of the address list

[[(11)]] can be read and stored in the data list [[(12)]] and/or the data stored in the data list [[(12)]] can be stored at the memory locations which are in the address space [[(10)]] of the control device microcontroller [[(3)]] and which are determined by the contents of the address list [[(11)]].

2. (Currently Amended) The [[A]]adjustment device according to claim 1, ~~characterized by the fact that~~ wherein the programmable unit [[(5)]] comprises the adjustment device debug interface [[(8)]].

3. (Currently Amended) The [[A]]adjustment device according to [[c]]Claim 1, ~~or 2, characterized by the fact that~~ wherein the programmable unit [[(5)]] is a programmable logic chip, ~~, in particular a field programmable gate array (FPGA).~~

4. (Currently Amended) The [[A]]adjustment device according to Claim1, ~~one of the claims 1 to 3, characterized by the fact that~~ wherein the memory [[(9)]] for the address list [[(11)]] and for the data list [[(12)]] is provided in the programmable unit [[(5)]].

5. (Currently Amended) The [[A]]adjustment device according to Claim 1, ~~one of the claims 1 to 4, characterized by the fact that~~ wherein the programmable unit [[(5)]] comprises a list application unit [[(13)]] and by activation of the list application unit [[(13)]] the list application unit [[(13)]] automatically carries out either the calling of the data from the memory

locations in the address space [[(10)]] of the control device microcontroller [[(3)]] and given in the address list [[(11)]] and the storing of the called data in the data list [[(12)]] or the writing of the data stored in the data list [[(12)]] into the memory locations in the address space [[(10)]] of the control device microcontroller [[(3)]] and determined by the contents of the address list [[(11)]].

6. (Currently Amended) The [[A]]adjustment device according to [[c]]Claim 5, ~~characterized by the fact that,~~ wherein in the case of several address lists [[(11)]] and/or several data lists [[(12)]], by issuing priorities for the address lists [[(11)]]and/or data lists [[(12)]] a processing order can be determined by the list application unit [[(13)]].

7. (Currently Amended) The [[A]]adjustment device according to Claim 5, ~~claim 5 or 6, characterized by the fact that~~ wherein in the case of several address lists [[(11)]] and/or several data lists [[(12)]] a subset of address lists [[(11)]] and/or a subset of data lists [[(12)]] can be determined which is processed by the list application unit [[(13)]].

8. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 1 to 7, characterized by the fact that~~ Claim 1, wherein the programmable unit [[(5)]] comprises an individual application unit [[(14)]] with which any memory locations in the address space [[(10)]] of the control device microcontroller [[(3)]] can be read out and/or with which a value can be stored in any memory location in the address space [[(10)]] of the control device microcontroller [[(3)]].

9. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 1 to 8, characterized by the fact that~~ Claim 1, wherein the programmable unit (5) comprises a tool interface unit (15) for connecting at least one external device (16) to the adjustment device (1).

10. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 1 to 9, characterized by the fact that~~ Claim 1, wherein the programmable unit [[(5)]] comprises a bypass unit [[(17)]] with an associated single-port or dual-port bypass memory [[(18)]], an associated bypass interface [[(19)]] for connecting the bypass unit [[(17)]] and the bypass memory [[(18)]] to an external simulation unit [[(20)]], where data can be exchanged between the control device [[(2)]] and the simulation unit [[(20)]] with the use of the bypass memory [[(18)]] and the bypass unit [[(17)]] reading and writing bi-directionally.

11. (Currently Amended) The [[A]]adjustment device according to claim 10, ~~characterized by the fact that~~ wherein the programmable unit [[(5)]] comprises the bypass interface [[(19)]], where the bypass interface [[(19)]] ~~in particular realizes~~ uses a serial data transmission and is ~~preferably~~ embodied as an LVDS interface.

12. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 1 to 11, characterized by the fact that~~ Claim 1, wherein the programmable unit [[(5)]] comprises a prioritization and arbitration unit [[(21)]], where priorities can be assigned to the various units

~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]] via the prioritization and arbitration unit [[(21)]] and the prioritization and arbitration unit [[(21)]] determines, with the aid of the priorities assigned to the various units ~~(13, 14, 15, 17)~~, the order of execution by activation of the various units ~~(13, 14, 15, 17)~~ among themselves and establishes a data connection between the unit activated in each case and the control device [[(2)]].

13. (Currently Amended) The [[A]]adjustment device according to claim 12, ~~characterized by the fact that~~ wherein the priority of the bypass unit [[(17)]] is higher than the priority of the list application unit [[(13)]] and/or that the priority of the list application unit [[(13)]] is higher than the priority of the individual value application unit ~~(13) [sic]~~ and/or that the priority of the individual value application unit [[(14)]] is higher than the priority of the tool interface unit [[(15)]].

14. (Currently Amended) The [[A]]adjustment device according to claim 12, ~~characterized by the fact that~~ wherein the priority of the tool interface unit [[(15)]] is higher than all the other units.

15. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 1 to 14, characterized by the fact that~~ Claim 1, wherein, the adjustment device [[(1)]] comprises a coordination unit [[(22)]] which is connected via a coordination interface [[(23)]] to one or more of the units ~~(13, 14, 17)~~ of the programmable unit [[(5)]] and/or via the data transmission

interface [[(6)]] to the operating computer [[(7)]] and/or via the bypass interface [[(19)]] to the simulation unit [[(20)]] and/or to the bypass memory [[(18)]].

16. (Currently Amended) The [[A]]adjustment device according to claim 15, ~~characterized by the fact that~~ wherein the coordination unit [[(22)]] directs data or instructions coming from the operating computer [[(7)]] and/or from the simulation unit [[(20)]] to the addressed units ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]] for further processing and/or transmits the data coming from a unit ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]] to the operating computer [[(7)]] and/or the simulation unit [[(20)]].

17. (Currently Amended) The [[A]]adjustment device according to ~~claim 15 or 16, characterized by the fact that~~ Claim 15, wherein the coordination unit [[(22)]] provides received data with a time stamp~~, in particular, data~~ which are transmitted to the operating unit [[(7)]].

18. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 15 to 17, characterized by the fact that~~ Claim 15, wherein the coordination unit [[(22)]] interprets configuration instructions coming from the operating unit [[(7)]] and/or from the simulation unit [[(20)]] and configures the adjustment device [[(1)]] accordingly.

19. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 15 to 18, characterized by the fact that~~ Claim 15, wherein the coordination unit [[(22)]] registers

external trigger signals [[(24)]] and/or internal trigger signals [[(25)]] and activates corresponding units ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]].

20. (Currently Amended) The [[A]]adjustment device according to ~~one of claims 15 to 19, characterized by the fact that~~ Claim 15, wherein the coordination unit [[(22)]] is ~~realized~~ located ~~either by~~ in a separate computer unit outside of the programmable unit [[(5)]], ~~in particular by~~ in a microcontroller, ~~or by~~ in a programmable logic chip, or is formed as a part of the programmable unit [[(5)]].

21. (Currently Amended) A [[P]]process for ~~the adjustment of~~ adjusting a control device with an adjustment device having at least one control device microcontroller, with at least one control device debug interface, at least one programmable unit, at least one data transmission interface for connecting the adjustment device to an operating unit, at least one adjustment device debug interface for connecting the adjustment device to the control device debug interface of the control device, at least one memory for at least one address list and at least one data list, wherein the programmable unit comprises a bypass unit with an associated single-port or dual-port bypass memory, an associated bypass interface for connecting the bypass unit and the bypass memory to an external simulation unit ~~according to one of claims 10 to 20, characterized by the fact that~~ comprising:

bypassing ~~of~~ at least one control device function ~~is carried out~~ by a corresponding bypassing function on the simulation unit [[(20)]] using, at least in part, the address list [[(11)]] and/or the data list [[(12)]].

22. (Currently Amended) The [[P]]process according to claim 21, ~~characterized by the fact that~~ wherein

the memory locations of the data necessary for the calculation of the bypass function are stored in the address space [[(10)]] of the control device microcontroller [[(3)]] in the address list [[(11)]],

the adjustment device [[(1)]] automatically carries out the reading of the data from the memory locations which are given in the address list [[(11)]] and are located in the address space [[(10)]] of the control device microcontroller [(3)]] and the storing of the called data in the data list ~~(12), in particular~~ with the use of the list application unit [[(13)]],

the data stored in the data list [[(12)]] are transmitted automatically, or on request by the simulation unit [[(20)]], to the simulation unit [[(20)]],

the results of the calculation of the bypass function by the simulation unit [[(20)]] are then transmitted to the adjustment device [[(1)]] and stored there either in the data list [[(12)]] and/or the bypass memory [[(18)]], and

the results of the calculation of the bypass function from the data list [[(12)]] and/or the bypass memory [[(18)]], where those results are stored in the adjustment device [[(1)]], are stored in certain memory locations in the address space [[(10)]] of the control device microcontroller [[(3)]], where the memory locations are ~~either~~ already stored in the address list [[(11)]] or are transmitted by the simulation unit ~~(20), in particular~~ with the results of the calculation of the bypass function.

23. (Currently Amended) The [[P]]process according to ~~one of the claims 21 or 22, where~~ Claim 21, wherein the adjustment device [[(1)]] comprises a coordination unit [[(22)]], characterized by the fact that the coordination unit [[(22)]] directs data or instructions coming from the operating computer [[(7)]] and/or from the simulation unit [[(20)]] to the addressed units ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]] for further processing and/or transmits the data coming from a unit ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]] to the operating computer [[(7)]] and/or the simulation unit [[(20)]].

24. (Currently Amended) The [[P]]process according to claim 23, ~~characterized by the fact that~~ wherein the coordination unit [[(22)]] provides received data with a time stamp~~, in particular data~~ which are transmitted to the operating unit [[(7)]].

25. (Currently Amended) The [[P]]process according to ~~one of the claims 23 or 24, characterized by the fact that~~ Claim 23, wherein the coordination unit [[(22)]] interprets configuration instructions coming from the operating unit [[(7)]] and/or from the simulation unit [[(20)]] and configures the adjustment device [[(1)]] accordingly.

26. (Currently Amended) The [[P]]process according to ~~one of the claims 23 to 25, characterized by the fact that that~~ Claim 23, wherein the coordination unit [[(22)]] registers external trigger signals [[(24)]] and/or internal trigger signals [[(25)]] and activates corresponding units ~~(13, 14, 15, 17)~~ of the programmable unit [[(5)]].